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| 10/597,306 | 07/19/2006 | Yoshifumi Kanetaka | NEC 04P199 | 9113 |

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| EXAMINER | |
|---|---|
| NORRIS, JEREMY C | |
| ART UNIT | PAPER NUMBER |
| 2841 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/597,306 | KANETAKA ET AL. | |
| | Examiner | Art Unit | |
| | Jeremy C. Norris | 2841 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/06,11/08,4/27/09,4/30/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Drawings*

Figures 1A-3C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Specification*

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it is too long. Correction is required. See MPEP § 608.01(b). Additionally, the Examiner notes that Applicant has supplied an abstract form PCT WO 2005/074338 A1, however, there is no corresponding instruction that this is intended to replace the abstract of 19 July 2006. Thus the 19 July 2006 abstract remains the abstract of record and is the basis of the objection. Moreover, the Examiner notes that the abstract of PCT WO 2005/074338 A1 would be acceptable if submitted as a replacement to the 19 July 2006 abstract.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 11-219762 (Sony).

Sony discloses, referring primarily to figures 3 and 4, a circuit board (4) having a plurality of through holes (25) into which a plurality of leads (12) of an electronic device are inserted and soldered (14): wherein a volume of a through hole (25a) of said through holes, into which an outermost end lead of said leads of said electronic device is inserted, is larger than a volume of a through hole of said through holes, into which a lead of said leads, which is located at a position nearest to a center of said electronic device, is inserted [claim 1], wherein a plane shape of each of said through holes is a circle, and wherein a diameter of said through hole, into which said outermost end lead of said electronic device is inserted, is larger than a diameter of said through hole, into which said lead at the position nearest to the center of said electronic device is inserted [claim 2].

Additionally, Sony discloses, a circuit board having a plurality of through holes (25) into which a plurality of leads (12) of an electronic device (11) are inserted and soldered: wherein a plane shape of a through hole of said through holes, into which a lead of said leads which is located at a position nearest to a center of said electronic device is inserted, is a circle, wherein a plane shape of a through hole of said through holes, into which an outermost end lead of said leads of said electronic device is inserted, is an ellipse having a major axis in a direction parallel with a line that connects

a center of the corresponding through hole and a center position of said electronic device at a time of being mounted, and wherein a length of the major axis of said ellipse is longer than a diameter of said through hole, into which said lead at the position nearest to the center of said electronic device is inserted (hole 25a is an ellipse of eccentricity=0 and since the diameter of 25a is larger than the diameter of 25, the limitation of the claim are met) [claim 4].

Moreover, Sony discloses, a circuit board (24) having a plurality of through holes (25) into which a plurality of leads (12) of an electronic device (11) are inserted and soldered: wherein a size of a through hole (25a) of said through holes, into which an outermost end lead of said leads of said electronic device is inserted, the size being measured in a direction of a line that connects a position of said outermost end lead of said electronic device being mounted before being soldered and a center position of said electronic device at a time of being mounted, is larger than a size of a through hole of said through holes, into which a lead of said leads which is located at the position nearest to the center of said electronic device is inserted, the size being measured in any direction in a plane [claim 5].

Regarding claim 6, the limitation “wherein an opening of said through hole into which said outermost end lead of said electronic device is inserted is formed by drilling more than once or by moving a drill relative to the board.” Is a process limitation in a product claim and thus has only been consider to the extent to which said process impacts the structure of said device, since it has been held “even though product-by-process claims are limited by and defined by the process, determination of patentability

is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe,* 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sony.

Sony discloses the claimed invention as described above except Sony does not specifically disclose that the diameter of said through hole, into which said outermost end lead of said electronic device is inserted, is not more than twice the diameter of said through hole, into which said lead at the position nearest to the center of said electronic device is inserted [claim 3]. However, it is well within the skill of the ordinary artisan to adjust the size of a hole of which fact the Examiner takes Official Notice. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the diameter of said through hole, into which said outermost end lead of said electronic device is inserted, is not more than twice the diameter of said through hole, into which said lead at the position nearest to the center of said electronic device is inserted in the invention of Sony as is known in the art. The motivation for doing so would have been to accommodate a lager pin that is not twice the diameter of the other pins.

Claims 1, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP Laid Open 12375/81 (Mitsumi) over Sony.

Mitsumi discloses referring primarily to figures 3 and 4, a circuit board (11) having a plurality of through holes (12) into which a plurality of leads (4) of an electronic device (3) are inserted: wherein a volume of a through hole (12d) of said through holes, into which an outermost end lead of said leads of said electronic device is inserted, is

larger than a volume of a through hole of said through holes, into which a lead of said leads, which is located at a position nearest to a center of said electronic device, is inserted. Mitsumi does not specifically disclose that the leads are soldered [claim 1]. However, It is well known in the art to solder leads into holes as evidenced by Sony. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to solder the leads to the holes in the invention of Mitsumi as is known in the art and evidenced by Sony. The motivation for doing so would have been to ensure a reliable electromechanical connection.

Additionally, the modified invention of Mitsumi teaches wherein shapes of through holes (12b, 12c) of said through holes, which are located between said through hole (12a), into which said lead at the position nearest to the center of said electronic device is inserted, and said through hole (12d), into which said outermost end lead of said electronic device is inserted, are gradually changed from a shape of said through hole into which said lead at the position nearest to the center of said electronic device is inserted to a shape of said through hole into which said outermost end lead of said electronic device is inserted [claim 7] , wherein a center position of said through hole into which said outermost end lead of said electronic device is inserted is shifted in a direction away from a center position of said electronic device at the time of being mounted, from a position of said outermost end lead of said electronic device, which is mounted before being soldered, when a thermal expansion coefficient of said electronic device is larger than a thermal expansion coefficient of said circuit board, and the center position is shifted in a direction approaching a center of said electronic device at the

time of being mounted, from a position of said outermost end lead of said electronic device, which is mounted before being soldered, when the thermal expansion coefficient of said electronic device is smaller than the thermal expansion coefficient of said circuit board (figure 4) [claim 8].

Similarly, Mitsumi discloses, a circuit board (11) having a plurality of through holes into which a plurality of leads (4) of an electronic device (3) are inserted: wherein a center position of a through hole (12d) of said through holes, into which an outermost end lead of said leads of said electronic device is inserted, is shifted in a direction away from a center position of said electronic device at the time of being mounted, from a position of said outermost end lead of said electronic device, which is mounted before being soldered, when a thermal expansion coefficient of said electronic device is larger than a thermal expansion coefficient of said circuit board, and the center position is shifted in a direction approaching a center of said electronic device at a time of being mounted, from the position of said outermost end lead of said electronic device, which is mounted before being soldered, when the thermal expansion coefficient of said electronic device is smaller than the thermal expansion coefficient of said circuit board. Mitsumi does not specifically disclose that the leads are soldered [claim 9]. However, It is well known in the art to solder leads into holes as evidenced by Sony. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to solder the leads to the holes in the invention of Mitsumi as is known in the art and evidenced by Sony. The motivation for doing so would have been to ensure a reliable electromechanical connection.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is (571)272-1932. The examiner can normally be reached on Monday - Thursday, 8:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeremy C. Norris
Primary Examiner
Art Unit 2841

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Primary Examiner, Art Unit 2841